Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An improved binary decoder, comprising:

selection means for activating from a plurality of outputs a single selected output corresponding to an input binary value, and

deselecting means coupled to the plurality of outputs that utilizes the single selected output to deactivate ~~the plurality of~~ nonselected outputs ~~except the selected output~~ when the single selected output is activated by forcing the nonselected output to a reference potential.

2. (Original) The improved binary decoder of claim 1, wherein the selection means comprises a circuit arrangement of gates for selecting a desired output.

3. (Currently Amended) The improved binary decoder of claim 1, wherein the deselecting means comprises a circuit arrangement having a single input connected to the selected output of the selection means, and a plurality of outputs each of which is connected to one of the remaining outputs of the selection means, such that when the input of the circuit arrangement is active all the other outputs of the decoder are forced to the inactive state by coupling the nonselected outputs to the reference potential.

4. (Currently Amended) A method for providing an improved binary decoder, comprising the steps of:

providing selection means for activating from a plurality of outputs a single selected output corresponding to an input binary value, and

providing a deselecting means coupled to the plurality of outputs that utilizes the single selected output to deactivate ~~the plurality of~~ nonselected outputs of the selection means ~~except the selected output~~ when the single selected output is activated.

5. (Previously Presented) A binary decoder, comprising:

a first pair of parallel-coupled transistors and a second pair of parallel-coupled transistors, the first and second pair of parallel-coupled transistors coupled between a voltage source and first and second outputs, respectively;

a third transistor coupled between the first output and a reference potential, and a fourth transistor coupled between the second output and the reference potential; and

the first and second pair of parallel-coupled transistors each having an input terminal, and the third and fourth transistors each having an input terminal, the first output coupled to a first input of the second pair of parallel-coupled transistors, the second output coupled to a first input of the second pair of parallel-coupled transistors.

6. (Previously Presented) The decoder of claim 5, wherein the input terminals of the first and second pair of parallel-coupled transistors are each configured to receive a compliment of a first input signal, the input terminal of the third transistor configured to receive the compliment of a second input signal and the input terminal of the fourth transistor configured to receive the uncomplimented first input signal.

7. (Previously Presented) The decoder of claim 5, wherein the input terminals of the first and second pair of parallel-coupled transistors are each configured to receive the uncomplimented input of a first input signal, the third transistor having its input terminal configured to receive the compliment of a second input signal, and the fourth transistor having its input terminal configured to receive the uncomplimented second input signal.

8. (Previously Presented) A decoder for integrated circuits, comprising:

a first set of parallel-coupled transistors coupled between a voltage source and a first output and comprising first, second, and third transistors, each having respective inputs;

a second set of parallel-coupled transistors coupled between the voltage source and a second output, the second set of parallel-coupled transistors comprising fourth, fifth, and sixth transistors, each having respective inputs;

a seventh transistor coupled between the first output and a common node and having an input, an eighth transistor coupled between the second output and the common node and having an input, and a ninth transistor coupled between the common node and a voltage reference and having an input.

9. (Previously Presented) The decoder of claim 8, wherein the input of the first transistor is coupled to the second output, the input of the third transistor is coupled to the second output, the input of the seventh transistor is configured to receive an uncomplimented first input signal, the input of the eighth transistor is configured to receive the compliment of the first input signal, the input of the second transistor configured to receive the compliment of a second input signal, the input of the third transistor configured to receive the compliment of a third input signal, the input of the fifth transistor configured to receive the compliment of the second input signal, the input of the sixth transistor configured to receive the compliment of the third input signal, the input of the ninth transistor configured to receive the compliment of the second input signal, and the reference potential set to the uncomplimented third input signal.

10. (Previously Presented) The decoder of claim 8, wherein the first and second outputs are set to active low.

11. (Previously Presented) The decoder of claim 8, wherein the input of the first transistor is coupled to the second output, the input of the fourth transistor is coupled to the first output, the input of the seventh transistor is configured to receive an uncomplimented first input signal, the input of the eighth transistor configured to receive the compliment of the first

input signal, the input of the second transistor configured to receive the compliment of the second input signal, the input of the third transistor configured to receive an uncomplimented third input signal, the input of the fifth transistor configured to receive the compliment of the second input signal, the input of the sixth transistor configured to receive the uncomplimented third input signal, the input of the ninth transistor configured to receive the complimented input of the second input signal, and the reference potential set to the complimented third input signal.

12. (Previously Presented) The decoder of claim 8, wherein the input of the first transistor is coupled to the second output, the input of the fourth transistor is coupled to the first output, the input of the seventh transistor is coupled to an uncomplimented first input signal, the input of the ninth transistor is coupled to an uncomplimented second input signal, the input of the second transistor is coupled to a complimented third input signal, the third transistor is coupled to an uncomplimented second input signal, the fifth transistor is coupled to the second uncomplimented input signal, the sixth transistor is coupled to the complimented third input signal, and the ground reference is set to the uncomplimented third input signal.

13. (Previously Presented) The decoder of claim 8, wherein the input of the first transistor is coupled to the second output, the input of the fourth transistor is coupled to the first input, the input of the seventh transistor is coupled to an uncomplimented first input signal, the input of the second transistor is coupled to an uncomplimented second input signal, the input of the third transistor is coupled to an uncomplimented third input, the input of the fifth transistor is coupled to the uncomplimented second input signal, the input of the sixth transistor is coupled to the uncomplimented third input signal, the input of the eighth transistor is coupled to the complimented first input signal, the input of the ninth transistor is coupled to the uncomplimented second input signal, and the reference voltage set to the complimented third input signal.

14. (Previously Presented) The decoder of claim 8, wherein the first and second pair of parallel-coupled transistors comprises PMOS transistors, and the third and fourth transistors comprise NMOS transistors.

15. (Currently Amended) A binary decoder, comprising:

a selection circuit structured to activate from a plurality of outputs a single selected output corresponding to an input binary value; and

a deselecting circuit coupled to the plurality of outputs that utilizes the single selected output to deactivate ~~the plurality of~~ nonselected outputs ~~except the selected output~~ when the single selected output is activated by forcing the nonselected outputs to a reference voltage.

16. (Previously Presented) The binary decoder of claim 15, wherein the selection circuit comprises an arrangement of gates for selecting a desired output.

17. (Currently Amended) The decoder of claim 15, wherein the deselecting circuit comprises a single input connected to the selected output of the selection circuit, and a plurality of outputs, each of which is connected to one of the remaining outputs of the selection circuit such that when the single input of the deselection circuit is active, ~~all the other~~ nonselected outputs of the decoder are forced to an inactive state by coupling to the reference voltage.

18. (Previously Presented) The decoder of claim 15, wherein the selection and deselection circuits are connected to provide a 2-to-4 decoder that provides an active low output for an input of A'.B' and for an input A.B'.

19. (Previously Presented) The decoder of claim 15, wherein the selection and deselection circuits are connected to provide a 2-to-4 decoder that provides an active low output for an input of A'.B and for an input A.B.

20. (Previously Presented) The decoder of claim 15, wherein the selection and deselection circuits are connected to provide a 3-to-8 decoder that provides an active low output for an input of A'.B'.C' and for an input A.B'.C'.

21. (Previously Presented) The decoder of claim 15, wherein the selection and deselection circuits are connected to provide a 3-to-8 decoder that provides an active low output for an input of A'.B'.C and for an input A.B'.C.

22. (Previously Presented) The decoder of claim 15, wherein the selection and deselection circuits are connected to provide a 3-to-8 decoder that provides an active low output for an input of A'.B.C' and for an input A.B.C'.

23. (Previously Presented) The decoder of claim 15, wherein the selection and deselection circuits are connected to provide a 3-to-8 decoder that provides an active low output for an input A'.B.C and for an input A.B.C.

24. (Currently Amended) The decoder of claim 15, wherein the selection circuit includes:

a first transistor coupled between a reference voltage and a first one of the outputs; and

a second transistor coupled between the reference voltage and a second one of the outputs, wherein the deselection circuit includes:

a third transistor connected between ~~the reference~~ a voltage source and the first output and having ~~an input~~ a control terminal connected to the second output: and

a fourth transistor connected between ~~the reference~~ a voltage source and the second output having ~~an input~~ a control terminal connected to the first output.

25. (New) The decoder of claim 24, wherein the selection circuit includes a fifth transistor coupled between the voltage source and the first output and a control terminal

coupled to a first input terminal, and a sixth transistor coupled between the voltage source and the second output and a control terminal coupled to a second input terminal.